Description

DISPLAY DEVICE

Technical Field

[1] The present invention relates to a display device.

Background Art

[2] Recently, flat panel displays such as organic light emitting displays, plasma display panels, and liquid crystal displays are widely developed.

[3] The liquid crystal display (LCD) is a representative of the flat panel displays. The LCD includes a liquid crystal (LC) panel assembly including two panels provided with two kinds of field generating electrodes such as pixel electrodes and a common electrode and a LC layer with dielectric anisotropy interposed therebetween. The variation of the voltage difference between the field generating electrodes, i.e., the variation in the strength of an electric field generated by the electrodes changes the transmittance of the light passing through the LCD, and thus desired images are obtained by controlling the voltage difference between the electrodes.

[4] The LCD includes a plurality of pixels including three sub-pixels representing red, green and blue colors.

[5] However, the three primary color system has a limit in color reproductivity for some ranges of colors. In detail, the commercially available display device can represent the colors determined by NTSC (national television system committee) or EBU (European broadcasting union). However, the colors determined by NTSC or EBU occupy only about 90% of natural colors and thus remaining 10% colors cannot be correctly represented. In particular, the LCD represents only 70% of the colors determined by NTSC.

Disclosure of Invention

Technical Problem

[6] A motivation of the present invention is to solve the problems of the conventional technique.

Technical Solution

[7] A display device is provided, which includes: a plurality of pixels arranged in matrix, each pixel including a first set of three primary color subpixels and at least one of a second set of three primary color subpixels, wherein the first and the second sets of three primary colors have a complementary relation.

[8] The subpixels in each pixel may be arranged in a 2×2 matrix.

[9] The first set of three primary color subpixels may include red, green, and blue subpixels, and the second set of three primary color subpixels may include cyan, magenta, and yellow subpixels.

[10] The red and the blue subpixels may be arranged in a row and the red and the green subpixels may be arranged in a column.

[11] A display device is provided, which includes: a plurality of pixels arranged in mat rix, each pixel including first to third pairs of subpixels, wherein the first pair of subpixels are disposed adjacent to each other, the second and the third sets of subpixels are disposed opposite each other with respect to the first pair of subpixels, and the first to the third sets of subpixels include first-color subpixels and second-color subpixels.

[12] Each subpixel in the first pair of subpixels may be triangular, and the first pair of subpixels may form a diamond.

[13] A boundary between the first pair of subpixels may extend in a row or column direction.

[14] The first-color and the second-color subpixels may have complementary relation.

[15] The first-color subpixels may include red, green, and blue subpixels, and the second-color subpixels may include cyan, magenta, and yellow subpixels.

[16] The first-color subpixels may include red, green, and blue subpixels and the second-color subpixels may include cyan, white, and yellow subpixels.

[17] A display device is provided, which includes: a matrix of pixels, each pixel including a pair of central subpixels adjacent to each other, a pair of first subpixels, and a pair of second subpixels, the pairs of first and second subpixels disposed in diagonals with respect to the central subpixels; a plurality of gate lines extending in a row direction and transmitting gate signals; and a plurality of data lines extending in a column direction and transmitting data signals, wherein each subpixel includes a pixel electrode and a thin film transistor, the subpixels include first and second sets of three primary color subpixels, and the first and the second sets of three primary color subpixels have complementary relation.

[18] Each of the central subpixels may be isosceles triangular and the central subpixels may form a diamond.

[19] A boundary between the central subpixels may extend in a row or column direction.

[20] The first set of three primary color subpixels may include red, green, and blue subpixels, and the second set of three primary color subpixels may include cyan, magenta, and yellow subpixels.

Advantageous Effects

[21] The multi-color configuration including at least one color in addition to red, green, and blue colors increases the reproductivity of colors.

Brief Description of the Drawings

[22] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawing in which:

[23] Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention;

[24] Fig. 2 is an equivalent circuit diagram of a subpixel of an LCD according to an embodiment of the present invention;

[25] Fig. 3 shows arrangements of four four-color subpixels of an LCD according to embodiments of the present invention.

[26] Fig. 4 is a layout view of a TFT array panel according to an embodiment of the present invention;

[27] Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V';

[28] Figs. 6 and 7 show arrangements of six six-color subpixels of an LCD according to embodiments of the present invention;

[29] Fig. 8 is an exemplary layout view of a TFT array panel for an LCD having the subpixel configuration shown in Fig. 6;

[30] Fig. 9 is an exemplary layout view of a TFT array panel for an LCD having the subpixel configuration shown in Fig. 7;

[31] Fig. 10 is a sectional view of the TFT array panel shown in Fig. 9 taken along the line X-X';

[32] Fig. 11 illustrates a color coordinate system; and

[33] Fig. 12 is a table illustrating the thickness of magenta color filters in unit of microns, color coordinates, and relative luminance.

Best Mode for Carrying Out the Invention

[34] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown.

[35] In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being on another element, it can be directly on the other element or intervening elements may also be present. In contrast,

when an element is referred to as being directly on another element, there are no intervening elements present.

[36] Fig. 1 is a block diagram of an LCD according to an embodiment of the present invention, and Fig. 2 is an equivalent circuit diagram of a subpixel of an LCD according to an embodiment of the present invention.

[37] Referring to Fig. 1, an LCD according to an embodiment includes a LC panel assembly 300, a gate driver 400 and a data driver 500 that are connected to the panel assembly 300, a gray voltage generator 800 connected to the data driver 500, and a signal controller 600 controlling the above elements.

[38] Referring to Fig. 1, the panel assembly 300 includes a plurality of display signal lines G_1-G_n and D_1-D_m and a plurality of subpixels connected thereto and arranged substantially in a matrix. In a structural view shown in Fig. 2, the panel assembly 300 includes lower and upper panels 100 and 200 and a LC layer 3 interposed therebetween.

[39] The display signal lines G_1-G_n and D_1-D_m are disposed on the lower panel 100 and include a plurality of gate lines G_1-G_n transmitting gate signals (also referred to as scanning signals), and a plurality of data lines D_1-D_m transmitting data signals. The gate lines G_1-G_n extend substantially in a row direction and substantially parallel to each other, while the data lines D_1-D_m extend substantially in a column direction and substantially parallel to each other.

[40] Each subpixel includes a switching element Q connected to the signal lines G_1-G_n and D_1-D_m, and a LC capacitor C_{LC} and a storage capacitor C_{ST} that are connected to the switching element Q. If unnecessary, the storage capacitor C_{ST} may be omitted.

[41] The switching element Q including a TFT is provided on the lower panel 100 and has three terminals: a control terminal connected to one of the gate lines G_1-G_n; an input terminal connected to one of the data lines D_1-D_m; and an output terminal connected to both the LC capacitor C_{LC} and the storage capacitor C_{ST}.

[42] The LC capacitor C_{LC} includes a pixel electrode 190 provided on the lower panel 100 and a common electrode 270 provided on an upper panel 200 as two terminals. The LC layer 3 disposed between the two electrodes 190 and 270 functions as dielectric of the LC capacitor C_{LC}. The pixel electrode 190 is connected to the switching element Q, and the common electrode 270 is supplied with a common voltage Vcom and covers an entire surface of the upper panel 200. Unlike Fig. 2, the common electrode 270 may be provided on the lower panel 100, and both electrodes 190 and 270 may have shapes of bars or stripes.

[43] The storage capacitor C_{ST} is an auxiliary capacitor for the LC capacitor C_{LC}. The storage capacitor C_{ST} includes the pixel electrode 190 and a separate signal line, which is provided on the lower panel 100, overlaps the pixel electrode 190 via an insulator, and is supplied with a predetermined voltage such as the common voltage Vcom. Alternatively, the storage capacitor C_{ST} includes the pixel electrode 190 and an adjacent gate line called a previous gate line, which overlaps the pixel electrode 190 via an insulator.

[44] For color display, each subpixel uniquely represents one of primary colors (i.e., spatial division) or each subpixel sequentially represents the primary colors in turn (i.e., temporal division) such that spatial or temporal sum of the primary colors are recognized as a desired color. Fig. 2 shows an example of the spatial division that each subpixel includes a color filter 230 representing one of the primary colors in an area of the upper panel 200 facing the pixel electrode 190. Alternatively, the color filter 230 is provided on or under the pixel electrode 190 on the lower panel 100.

[45] An example of a set of the primary colors includes first three primary colors including red, green, and blue colors and at least one of second three primary colors complementary to the first three primary colors, i.e., cyan, magenta, and yellow colors. However, magenta may be substituted with white or transparency.

[46] One or more polarizers (not shown) are attached to at least one of the panels 100 and 200.

[47] Referring to Fig. 1 again, the gray voltage generator 800 generates two sets of a plurality of gray voltages related to the transmittance of the subpixels. The gray voltages in one set have a positive polarity with respect to the common voltage Vcom, while those in the other set have a negative polarity with respect to the common voltage Vcom.

[48] The gate driver 400 is connected to the gate lines G_1-G_n of the panel assembly 300 and synthesizes the gate-on voltage Von and the gate-off voltage Voff from an external device to generate gate signals for application to the gate lines G_1-G_n.

[49] The data driver 500 is connected to the data lines D_1-D_m of the panel assembly 300 and applies data voltages, which are selected from the gray voltages supplied from the gray voltage generator 800, to the data lines D_1-D_m.

[50] The drivers 400 and 500 may include at least one integrated circuit (IC) chip mounted on the panel assembly 300 or on a flexible printed circuit (FPC) film in a tape carrier package (TCP) type, which are attached to the LC panel assembly 300. Alternately, the drivers 400 and 500 may be integrated into the panel assembly 300 along

with the display signal lines G_1-G_n and D_1-D_m and the TFT switching elements Q.

[51] The signal controller 600 controls the gate driver 400 and the gate driver 500.

[52] Now, the operation of the above-described LCD will be described in detail.

[53] The signal controller 600 is supplied with input three-color image signals R, G and B and input control signals controlling the display thereof such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a main clock MCLK, and a data enable signal DE, from an external graphics controller (not shown). After generating gate control signals CONT1 and data control signals CONT2 and converting and processing the input image signals R, G and B into multi-color image signals R', G', B' and CC suitable for the operation of the panel assembly 300 on the basis of the input control signals and the input image signals R, G and B, the signal controller 600 transmits the gate control signals CONT1 to the gate driver 400, and the processed image signals R', G', B' and CC and the data control signals CONT2 to the data driver 500. Reference numeral CC denotes an image signal for a subpixel representing at least one of the second three primary colors.

[54] The gate control signals CONT1 include a scanning start signal STV for instructing to start scanning and at least a clock signal for controlling the output time of the gate-on voltage Von. The gate control signals CONT1 may further include an output enable signal OE for defining the duration of the gate-on voltage Von.

[55] The data control signals CONT2 include a horizontal synchronization start signal STH for informing of start of data transmission for a group of subpixels, a load signal LOAD for instructing to apply the data voltages to the data lines D_1-D_m, and a data clock signal HCLK. The data control signal CONT2 may further include an inversion signal RVS for reversing the polarity of the data voltages (with respect to the common voltage Vcom).

[56] Responsive to the data control signals CONT2 from the signal controller 600, the data driver 500 receives a packet of the image data R', G', B' and CC for the group of subpixels from the signal controller 600, converts the image data R', G', B' and CC into analog data voltages selected from the gray voltages supplied from the gray voltage generator 800, and applies the data voltages to the data lines D_1-D_m.

[57] The gate driver 400 applies the gate-on voltage Von to the gate line G_1-G_n in response to the gate control signals CONT1 from the signal controller 600, thereby turning on the switching elements Q connected thereto. The data voltages applied to the data lines D_1-D_m are supplied to the subpixels through the activated switching elements Q.

[58] The difference between the data voltage and the common voltage Vcom is represented as a voltage across the LC capacitor C_{LC}, which is referred to as a subpixel voltage. The LC molecules in the LC capacitor C_{LC} have orientations depending on the magnitude of the subpixel voltage, and the molecular orientations determine the polarization of light passing through the LC layer 3. The polarizer(s) converts the light polarization into the light transmittance.

[59] By repeating this procedure by a unit of the horizontal period (which is denoted by 1H and equal to one period of the horizontal synchronization signal Hsync and the data enable signal DE), all gate lines G_1-G_n are sequentially supplied with the gate-on voltage Von during a frame, thereby applying the data voltages to all subpixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver 500 is controlled such that the polarity of the data voltages is reversed (which is referred to as frame inversion). The inversion control signal RVS may be also controlled such that the polarity of the data voltages flowing in a data line in one frame are reversed (for example, line inversion and dot inversion), or the polarity of the data voltages in one packet are reversed (for example, column inversion and dot inversion).

[60] In the meantime, a dot or a pixel that is a basic unit for displaying an image according to embodiments of the present invention includes red, green, and blue subpixels and at least one of cyan, magenta, and yellow subpixels. Generally, the colors are determined by dominant wavelength and the luminance of a color is determined by the intensity of the dominant wavelength. In this respect, the three brightest subpixels are yellow, cyan, and green subpixels in sequence, while blue subpixels are the darkest and red and magenta subpixels are intermediate.

[61] Now, subpixel arrangements of a pixel including four-color subpixels on the panel assembly according to embodiments of the present invention will be described in detail with reference to Fig. 3.

[62] Hereinafter, a subpixel is referred to as red, green, blue, cyan, magenta, and yellow subpixel depending on the color represented by the subpixel and the red, green, blue, cyan, magenta, and yellow subpixels are denoted by reference characters R, G, B, C, M, and Y, respectively, which also denote the image signals for the colors.

[63] Fig. 3 shows arrangements of four four-color subpixels of an LCD according to embodiments of the present invention.

[64] Referring to Fig. 3, the subpixels forming a pixel are arranged in a 2×2 matrix that includes a first row including red and blue subpixels R and B and a second row

including a green subpixel and one of cyan, magenta, and yellow subpixels C, M and Y (indicated by (a), (b), and (c), respectively). The 2×2 matrix is approximately square and each subpixel may be square.

[65] The arrangements shown in Fig. 3 are only examples of possible arrangements and the arrangements may be determined in consideration of complementary relation between the colors. The multi-color configuration including at least one color in addition to red, green, and blue colors increases the reproductivity of colors.

[66] Now, a lower panel, i.e., a TFT array panel for an LCD having a subpixel arrangement shown in Fig. 3 will be described in detail with reference to Figs. 4 and 5 as well as Fig. 2.

[67] Fig. 4 is a layout view of a TFT array panel according to an embodiment of the present invention, and Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V'.

[68] A plurality of gate lines 121 for transmitting gate signals are formed on an insulating substrate 110. Each gate line 121 extends substantially in a transverse direction and includes a plurality of gate electrodes 124 and a plurality of projections 127 protruding downward. Each gate line 121 may extend to be connected to a gate driver (not shown) that may be integrated on the substrate 110 or may have an end portion having a large area for contact with another layer or a gate driver that may be mounted on the substrate 110 or on an external device such as a flexible printed circuit (FPC) film (not shown), which may be attached to the substrate 110.

[69] The gate lines 121 are preferably made of Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy, Cu containing metal such as Cu and Cu alloy, Mo containing metal such as Mo and Mo alloy, Cr, Ti or Ta. The gate lines 121 may have a multi-layered structure including two films having different physical characteristics. One of the two films is preferably made of low resistivity metal including Al containing metal, Ag containing metal, and Cu containing metal for reducing signal delay or voltage drop in the gate lines 121 and the storage electrode lines 131. The other film is preferably made of material such as Mo containing metal, Cr, Ta or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two films are a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film.

[70] In addition, the lateral sides of the gate lines 121 are inclined relative to a surface of the substrate 110, and the inclination angle thereof ranges about 30-80 degrees.

[71] A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121.

[72] A plurality of semiconductor islands 154 preferably made of hydrogenated amorphous silicon (abbreviated as a-Si) or polysilicon are formed on the gate insulating layer 140. Each semiconductor island 154 is located on the gate electrodes 124.

[73] A plurality of ohmic contact islands 163 and 165preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor islands 154.

[74] The lateral sides of the semiconductor islands 154 and the ohmic contacts 163 and 165 are inclined relative to the surface of the substrate 110, and the inclination angles thereof are preferably in a range of about 30-80 degrees.

[75] A plurality of data lines 171, a plurality of drain electrodes 175, and a plurality of storage capacitor conductors 177 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.

[76] The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. Each data line 171 includes an end portion 179 having a larger area for contact with another layer or an external device such as a data driver.

[77] Each data line 171 includes a plurality of source electrodes 173 projecting toward the gate electrodes 124. Each pair of the source and drain electrodes 173 and 175 are separated from each other and disposed opposite each other with respect to a gate electrode 124. A gate electrode 124, a source electrode 173, and a drain electrode 175 along with a semiconductor island 154 form a TFT having a channel formed in the a semiconductor island 154 disposed between the source electrode 173 and the drain electrode 175.

[78] The storage capacitor conductors 177 overlap the projections 127 of the gate lines 121.

[79] The data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 are preferably made of refractory metal such as Mo containing metal, Cr, Ti, Ta or alloys thereof. However, they may also have a multilayered structure including a low-resistivity film (not shown) and a good-contact film (not shown). A good example of the combination is a lower Mo film, an intermediate Al film, and an upper Mo film as well as the above-described combinations of a lower Cr film and an upper Al-Nd alloy film and a lower Al film and an upper Mo film.

[80] Like the gate lines 121, the data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 have inclined edge profiles, and the inclination angles thereof range about 30-80 degrees.

[81] The ohmic contacts 161 and 165 are interposed only between the underlying semiconductor islands 154 and the overlying data lines 171 and the overlying drain electrodes 175 thereon and reduce the contact resistance therebetween. The semiconductor islands 154 include a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[82] A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, the storage electrode capacitors 177, and the exposed portions of the semiconductor stripes 151. The passivation layer 180 is preferably made of inorganic insulator such as silicon nitride and silicon oxide, photosensitive organic material having a good flatness characteristic, or low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD). The passivation layer 180 may have a double-layered structure including a lower inorganic film and an upper organic film.

[83] The passivation layer 180 has a plurality of contact holes 182, 185 and 187 exposing the end portions 179 of the data lines 171, the drain electrodes 175, and the storage conductors 177, respectively.

[84] A plurality of pixel electrodes 190 and a plurality of contact assistants 82, which are preferably made of ITO or IZO, are formed on the passivation layer 180.

[85] The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 185 and to the storage capacitor conductors 177 through the contact holes 187 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175 and transmit the received data voltages to the storage capacitor conductors 177.

[86] Referring to Fig. 2 again, the pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with a common electrode 270, which determine the orientations of liquid crystal molecules in a liquid crystal layer 3 disposed therebetween.

[87] As describe above, a pixel electrode 190 and a common electrode form a liquid crystal capacitor C_{LC}, which stores applied voltages after turn-off of the TFT. A storage capacitor C_{ST} for enhancing the voltage storing capacity is implemented by overlapping the pixel electrode 190 with the gate lines 121 adjacent thereto (called

previous gate lines). The capacitances of the storage capacitors, i.e., the storage capacitances are increased by providing the projections 127 at the gate lines 121 for increasing overlapping areas and by providing the storage capacitor conductors 177, which are connected to the pixel electrodes 190 and overlap the projections 127, under the pixel electrodes 190 for decreasing the distance between the terminals.

[88] The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase aperture ratio but it is optional.

[89] The contact assistants 82 are connected to the exposed end portions 179 of the data lines 171 through the contact holes 182. The contact assistants 82 protect the exposed portions 179 and complement the adhesion between the exposed portions 179 and external devices.

[90] According to another embodiment of the present invention, the pixel electrodes 190 are made of transparent conductive polymer. For a reflective LCD, the pixel electrodes 190 are made of opaque reflective metal. In these cases, the contact assistants 82 may be made of material such as ITO or IZO different from the pixel electrodes 190.

[91] Finally, an alignment layer 11 is coated on the surface of the substrate 110.

[92] Now, subpixel arrangements of a pixel including six-color subpixels on the panel assembly according to embodiments of the present invention will be described in detail with reference to Figs. 6 and 7.

[93] Figs. 6 and 7 show arrangements of six six-color subpixels of an LCD according to embodiments of the present invention.

[94] Referring to Figs. 6 and 7, the subpixels forming a pixel have an arrangement like a PenTile™ arrangement. The basic structure of the subpixel arrangement is a 2×2 matrix and a pair of isosceles triangle having a common bottom to form a diamond occupy the center of the 2×2 matrix. This configuration improves the image quality.

[95] In detail, first to fourth subpixels PX1-PX4 are arranged in two rows and two columns and fifth and sixth subpixels PX5 and PX6 are centered. The fifth and the sixth subpixels PX5 and PX6 shown in Fig. 6 are arranged in a column, while those shown in Fig. 7 are arranged in a row. Accordingly, the boundary between the fifth and the sixth subpixels PX5 and PX6 shown in Fig. 6 coincides with the boundary between subpixel rows, and that shown in Fig. 7 coincides with the boundary between subpixel columns.

[96] The arrangement of the colors is determined in consideration of the complementary relation and the color interference, etc.

[97] Now, TFT array panels for an LCD having subpixel arrangements shown in Figs. 6

and 7 will be described in detail with reference to Figs. 8-10.

[98] Fig. 8 is an exemplary layout view of a TFT array panel for an LCD having the subpixel configuration shown in Fig. 6, Fig. 9 is an exemplary layout view of a TFT array panel for an LCD having the subpixel configuration shown in Fig. 7, and Fig. 10 is a sectional view of the TFT array panel shown in Fig. 9 taken along the line X-X'.

[99] Referring to Figs. 8-10, a layered structure of the TFT array panel according to this embodiment is almost the same as those shown in Figs. 4 and 5.

[100] That is, a plurality of gate lines 121 including gate electrodes 124 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductors 154, and a plurality of ohmic contacts 163 and a plurality of ohmic contacts 165 are sequentially formed thereon. A plurality of data lines 171 including source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 are formed thereon. A plurality of contact holes 182 and 185 are provided at the passivation layer 180 and the gate insulating layer 140. A plurality of pixel electrodes 190 and a plurality of contact assistants 82 are formed on the passivation layer 180 and an alignment layer 11 is coated thereon.

[101] Different from the TFT array panel shown in Figs. 4 and 5, the TFT array panel according to this embodiment provides a plurality of storage electrode lines 131, which are separated from the gate lines 121, on the same layer as the gate lines 121 without providing projections at the gate lines 121. The storage electrode lines 131 are supplied with a predetermined voltage such as the common voltage. The storage electrode lines 131 include a plurality of diamond rings 133 and a plurality of projections 135 projecting from a midpoint of respective edges of the diamond rings 133. Without providing the storage capacitor conductors 177 shown in Figs. 4 and 5, and the drain electrodes 175 extend and expand to overlap the diamond rings 133 and the projections 135 of the storage electrode lines 131 to form storage capacitors.

[102] In addition, the semiconductors 154 and the ohmic contacts 163 extend along the data lines 171 to form semiconductor stripes 151 and ohmic contact stripes 161. The semiconductors 151 cover edges of the gate lines 121 and the storage electrodes 131, which meet the data lines 171 and the drain electrodes 175, to smooth surface profiles, thereby preventing the disconnection of the data lines 171 and the drain electrodes 175.

[103] The gate electrodes 124 project upward and downward and the source electrodes 173 are U or reversed U shaped

[104] Each of the pixel electrodes 190 are disposed on an area enclosed by the gate lines 121, the data lines 171, the diamond rings 133 of the storage electrode lines 131, or

imaginary transverse lines extending from the storage electrode lines 131. The drain electrodes 175 for the center subpixels PX5 and PX6 extend along the diamond rings 133 of the storage electrode lines 131 to be connected to respective pixel electrodes 190 near the midpoint of the edges of the diamond rings 133 or the corners of the diamond rings 133.

[105] Many of the above-described features of the TFT array panel for an LCD shown in Figs. 4 and 5 may be appropriate to the TFT array panel shown in Figs. 8-10.

[106] Now, the color reproductivity of the multi-color subpixel configuration will be described with reference to Fig. 11, which illustrates a color coordinate system.

[107] In Fig. 11, the areas denoted by reference characters A1, A2 and A3 indicate color ranges reproducible by red, green, blue colors, red, yellow, and green colors, and green, cyan, and blue colors, respectively.

[108] Accordingly, the addition of yellow and cyan colors to red, green, and blue colors increases the reproducible color range by the areas A2 and A3. It is noted that the addition of magenta may not significantly enlarge the reproducible color range. The substitution of magenta with white may increase the transmittance of light since the color filters 230 transmit only about one thirds of incident light.

[109] Now, the variation of the luminance depending on the variation of magenta will be described with reference to Fig. 12, which is a table illustrating the thickness of magenta color filters in unit of microns, color coordinates, and relative luminance. Here, it is noted that the variation of magenta is represented by the thickness of the magenta color filters since magenta color becomes strong as a magenta filter becomes thicker.

[110] The table shown in Fig. 12 shows that the luminance increases up to about 130% as the thickness of the magenta color filters becomes thin. Accordingly, the substitution of magenta with white further increases the luminance.

[111] The above description may be applicable to any display device such as a light emitting display or a plasma display panel.

[112] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

[113] **WHAT IS CLAIMED IS:**

[114]